JC07 Rec'd PCT/PTO 16 APR 2001

FORM PTO-1390 (REV 11-2000)	U S DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTORNEY'S DOCKET NUMBER 124-850
TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371		U.S APPLICATION NO (If known, see 37 C.F.R 1 5) 09/807515 Unknown
INTERNATIONAL APPLICATION NO. PCT/GB99/03428	INTERNATIONAL FILING DATE 22 October 1999	PRIORITY DATE CLAIMED 23 October 1998
TITLE OF INVENTION	IMPROVEMENTS IN IMPATT DIODES	
APPLICANT(S) FOR DO/EO/US	HERBERT et al.	

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. ☒ This is an express request to begin national examination procedures (35 U.S.C. 371(f). The submission must include items (5), (6), (9) and (21) indicated below.
4. ☒ The U.S. has been elected by the expiration of 19 months from the priority date (Article 31).
5. A copy of the International Application as filed (35 U.S.C. 371(c)(2)).
   a. ☐ is attached hereto (required only if not communicated by the International Bureau).
   b. ☒ has been communicated by the International Bureau.
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US).
6. ☐ An English language translation of the International Application as filed (35 U.S.C. 371(c)(2)).
   a. ☐ is attached hereto.
   b. ☐ has been previously submitted under 35 U.S.C. 154(d)(4).
7. ☒ Amendments to the claims of the International Application under PCT Article 34
   a. ☐ are attached hereto (required only if not communicated by the International Bureau).
   b. ☒ have been communicated by the International Bureau.
   c. ☐ have not been made; however, the time limit for making such amendments has **NOT** expired.
   d. ☐ have not been made and will not be made.
8. ☐ An English language translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).
9. ☒ An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)).
10. ☐ A English language translation of the annexes of the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)).

Items 11 To 20 below concern document(s) or information included:

11. ☐ An Information Disclosure Statement under 37 C.F.R. 1.97 and 1.98.
12. ☒ An assignment document for recording. A separate cover sheet in compliance with 37 C.F.R. 3.28 and 3.31 is included.
13. ☐ A FIRST preliminary amendment.
14. ☐ A SECOND or SUBSEQUENT preliminary amendment.
15. ☐ A substitute specification.
16. ☐ A change of power of attorney and/or address letter.
17. ☐ A computer-readable form of the sequence listing in accordance with PCT Rule 13ter.2 and 35 U.S.C. 1.821-1.825.
18. ☐ A second copy of the published international application under 35 U.S.C. 154(d)(4).
19. ☐ A second copy of the English language translation of the international application under 35 U.S.C. 154(d)(4).
20. ☒ Other items or information. PTO-1449/ International Search Report

516968

U.S. APPLICATION NO (if known, see 37 C.F.R 1.5)	INTERNATIONAL APPLICATION NO.	ATTORNEY'S DOCKET NUMBER
09/807515 Unknown	PCT/GB99/03428	124-850

21. ☒ The following fees are submitted:

	CALCULATIONS PTO USE ONLY
BASIC NATIONAL FEE (37 C.F.R. 1.492(a)(1)-(5):	
-- Neither international preliminary examination fee (37 C.F.R. 1.482) nor international search fee (37 C.F.R. 1.445(a)(2)) paid to USPTO and International Search Report not prepared by the EPO or JPO $1000.00	
-- International preliminary examination fee (37 C.F.R. 1.482) not paid to USPTO but International Search Report prepared by the EPO or JPO $860.00	
-- International preliminary examination fee (37 C.F.R. 1.482) not paid to USPTO but international search fee (37 C.F.R. 1.445(a)(2)) paid to USPTO $710.00	
-- International preliminary examination fee (37 C.F.R. 1.482) paid to USPTO but all claims did not satisfy provisions of PCT Article 33(1)-(4) $690.00	
-- International preliminary examination fee (37 C.F.R. 1.482) paid to USPTO and all claims satisfied provisions of PCT Article 33(1)-(4) $100.00	
ENTER APPROPRIATE BASIC FEE AMOUNT =	$ 860.00
Surcharge of $130.00 for furnishing the oath or declaration later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 C.F.R. 1.492(e)).	$ 0.00

CLAIMS	NUMBER FILED		NUMBER EXTRA	RATE			
Total Claims	20	-20 =	0	X	$18.00	$	0.00
Independent Claims	1	-3 =	0	X	$80.00		0.00
MULTIPLE DEPENDENT CLAIMS(S) (if applicable)					$270.00	$	270.00
					TOTAL OF ABOVE CALCULATIONS =	$	**1130.00**
☐ Applicant claims small entity status. See 37 CFR 1.27. The fees indicated above are reduced by 1/2.							0.00
					SUBTOTAL =	$	**1130.00**
Processing fee of $130.00, for furnishing the English Translation later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 C.F.R. 1.492(f)).					+		0.00
					TOTAL NATIONAL FEE =	$	**1130.00**
Fee for recording the enclosed assignment (37 C.F.R. 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 C.F.R. 3.28, 3.31). **$40.00** per property					+	$	40.00
Fee for Petition to Revive Unintentionally Abandoned Application ($1240.00 – Small Entity = $620.00)						$	0.00
					TOTAL FEES ENCLOSED =	$	**1170.00**
						Amount to be: refunded	$
						Charged	$

a. ☒ A check in the amount of $1170.00 to cover the above fees is enclosed.
b. ☐ Please charge my Deposit Account No. 14-1140 in the amount of $_____ to cover the above fees. A duplicate copy of this form is enclosed.
c. ☒ The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 14-1140. A duplicate copy of this form is enclosed.
d. ☒ The entire content of the foreign application(s), referred to in this application is/are hereby incorporated by reference in this application.

NOTE: Where an appropriate time limit under 37 C.F.R. 1.494 or 1.495 has not been met, a petition to revive (37 C.F.R. 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

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27,393 REGISTRATION NUMBER

April 16, 2001 Date

516968

Improvements in IMPATT Diodes

The present invention relates to semiconductor avalanche diodes, and in particular to IMPATT (impact ionisation avalanche transit time) diodes.

IMPATT diodes employ the impact-ionisation and transit time properties of semiconductor structures to produce negative resistance at microwave frequencies. An IMPATT diode consists of heavily doped n^{++} and p^{++} contact regions separated by a depleted region with a doping profile designed to produce an avalanche region and a drift region. The doping profile is designed to produce an avalanche region with a high electric field, sufficient to generate high multiplication levels by impact ionisation. The doping profile is designed to produce a drift region with an electric field sufficiently high to achieve carrier velocity saturation but sufficiently low to avoid impact ionisation.

A common example of an IMPATT diode has a lo-hi-lo doping profile in which the p^{++} contact region is followed by a n-type doped region, in which a first layer (adjacent to the p^{++} contact region) has a low doping concentration (n), a second layer has a high doping concentration (n^{+}) and a third layer has a low doping concentration (n). The first layer is the avalanche region and sustains a high electric field, the second layer is a doping spike to switch the electric field from a high value in the first layer to a lower value in the third layer, which is the drift region. The avalanche region of the diode will break down when the applied reverse bias voltage exceeds a threshold value.

Close to the breakdown voltage a rapid increase in current is caused by avalanche multiplication of holes and electrons in the avalanche region.

If an IMPATT device is mounted in a microwave cavity and a reverse bias voltage close to the breakdown voltage is applied, then the cavity can be tuned to allow the negative resistance of the diode to generate microwave oscillations with the diode voltage swinging above and below the breakdown voltage. When the rf voltage rises above zero (in its positive half cycle), an avalanche is initiated, a small number of holes and electrons arising from the reverse saturation current are greatly multiplied by the avalanche process. IMPATT diodes are normally designed so that the avalanche current peaks as the rf voltage approaches zero (towards the end of its positive half cycle). After passing through the avalanche region the electrons are swept into the low doped drift region and after a transit time delay the electrons are collected at the n^{++} contact region. Thus, the current resulting from the avalanche transits the drift region for the half period (negative half cycle) when the rf voltage is negative and this yields a negative resistance for rf current.

The IMPATT diode is one of the most powerful solid-state sources of microwave power. Continuous wave (CW) output powers as high as 10W at a few gigahertz and as high as 1W at 100GHz can be obtained from a single IMPATT diode device. However, IMPATT diodes are noisy and sensitive to operating conditions. The noise in an IMPATT diode arises mainly from the statistical nature of the generation rates of electron-hole pairs at and above the breakdown voltage. Noise can be reduced somewhat by operating an IMPATT diode well above the resonant frequency of the diode and keeping the current low. However, these conditions conflict with conditions favouring high power output and efficiency. Examples of IMPATT diodes are discussed in GB2,002,579 and EP757,392.

Partly, because of the high noise associated with IMPATT diodes, three terminal signal generators, such as transistors, are preferred at

microwave frequencies, with subsequent up-conversion and low noise amplification for higher frequencies. However, the high parasitics associated with three terminal structures indicates that two terminal devices, such as IMPATT diodes, would have a natural advantage at microwave and mm-wave frequencies if noise could be reduced.

MITTAT (mixed tunnelling avalanche transit time) IMPATT diodes are also known in which both tunnelling and ionisation effects are strong in the avalanche region, for example in EP262,346 and US5,466,965. This degrades efficiency as a significant proportion of the generated tunnel current undergoes little or no avalanche multiplication.

The present invention seeks to overcome some of the problems discussed above by providing an IMPATT diode which operates with much reduced noise levels.

According to a first aspect of the present invention there is provided an impact ionisation avalanche transit time (IMPATT) diode device comprising a main avalanche region and a drift region wherein the device additionally comprises a narrow bandgap region with a bandgap narrower than the bandgap in the main avalanche region which narrow bandgap region is located adjacent to the main avalanche region in order to generate within the narrow bandgap region a tunnel current which is injected into the main avalanche region. By incorporating a narrow bandgap region adjacent to the main avalanche region an injection tunnel current pulse can be generated in a predictable manner. This current pulse is injected into the main avalanche region where a low noise avalanche occurs.

Preferably, the narrow bandgap region is arranged to generate a tunnel current for injection into the main avalanche region at the peak reverse

bias voltage of an oscillating voltage applied across the terminals of the diode.

It is preferred that the narrow bandgap region is located at the edge of the main avalanche region.

The doping profile of an IMPATT diode according to the present invention must be designed to achieve an electric field across the narrow bandgap region of sufficient magnitude to provide the desired tunnel current amplitude at the peak reverse bias voltage For strained semiconductor materials such as Silicon Germanium/Silicon, a plurality of alternating narrow and wide bandgap layers may have to be used to form the narrow bandgap region in order to alleviate strain. However, in unstrained materials such as Galium Arsenide/Aluminium Gallium Arsenide, one narrow bandgap layer may be used to form the narrow bandgap region.

Most of the noise associated with a conventional IMPATT diode occurs due to the statistical nature of the generation of electron-hole pairs during the part of the positive half cycle of the oscillating voltage when the voltage is above the threshold breakdown voltage. The diode structure according to the present invention increases the predictability of electron-hole pairs being generated at voltages above the breakdown voltage and so can enable a low noise narrow pulse of current to be generated close to the time at which the oscillating bias becomes negative.

The IMPATT diode according to the present invention may have a single drift form, for example having a lo-hi-lo doping profile or a Misawa p-i-n doping profile. Alternatively, the diode according to the present invention may be a double drift diode. In a preferred embodiment of the present invention particularly suitable for a single drift diode the narrow

bandgap region is located between a heavily doped contact region and the main avalanche region so as to maximise the proportion of the avalanche region which can be used to multiply the electrons generated in the narrow bandgap material. In a preferred embodiment of the present invention particularly suitable for a double drift diode the narrow bandgap region may be located towards the centre of the avalanche region, so that both the n and p components of the tunnel current may undergo avalanche multiplication.

The IMPATT diode according to the present invention may be made of either III-V semiconductor materials, such as Gallium Arsenide/Aluminium Gallium Arsenide, or group IV semiconductor materials, such as Silicon Germanium/Silicon. The thickness of the narrow bandgap region and the composition of the alloys making up the narrow bandgap region are design parameters chosen to achieve the required tunnel current, as will be apparent to the person skilled in the art.

According to a further preferred embodiment of the present invention the length of the drift region (L_D) and the length of the avalanche region (L_A) are chosen such that the drift region is between 2 and 6 times, and more preferably between 3.5 and 4.5 times, the length of the avalanche region. This ensures that in the fundamental mode of oscillation, the period of oscillation (P) is between 4 and 12 times, and preferably close to 8 times (between 7.5 and 8.5 times), the avalanche region transit time (T_A). It has been found that this substantially reduces the noise generated by an IMPATT diode according to the present invention.

The IMPATT diode according to the present invention can be arranged such that at least part of the tunnel current is generated by optical excitation.

The present invention will now be described with reference to the following Figures in which:

Figure 1 shows the structure of a single drift IMPATT diode according to the present invention.

Figure 2 graphically illustrates the variation in conduction band and valence band edge energies along the IMPATT diode of Figure 1 showing injection by electron tunnelling.

Figure 3 graphically illustrates the variation in conduction band and valence band edge energies along the IMPATT diode of Figure 1 showing injection by optical excitation.

Figure 4 shows the variation of noise with multiplication factor for the device shown in Figure 2 for different periods of the fundamental mode of a generated voltage oscillation.

Figure 5 shows the tunnel current generated in the device of Figure 1 as a function of phase angle where the origin on the horizontal axis of the plot is chosen as 90°, i.e. at the positive peak of the voltage cycle.

Figure 6 shows the current waveform (I) generated in the device of Figure 1 by tunnelling and avalanche as a function of time.

Figure 7a shows the structure of a first embodiment of a double drift IMPATT diode according to the present invention.

Figure 7b graphically illustrates the variation in conduction band and valence band edge energies along the IMPATT diode of Figure 7a.

Figure 8a shows the structure of a second embodiment of a double drift IMPATT diode according to the present invention.

Figure 8b graphically illustrates the variation in conduction band and valence band edge energies along the IMPATT diode of Figure 8a.

Figure 9 shows the structure of a single drift IMPATT diode according to an alternative embodiment of the present invention.

The IMPATT diode (2) shown in Figure 1 is a lo-hi-lo type IMPATT diode, having a heavily doped p^{++} contact region (6), low doped semiconductor regions (8), (10) and (12) and a heavily doped n^{++} contact region (14). However, according to the present invention a narrow band gap region (4) is located between the low doped region (8) and the low doped region (10).

The material compositions, layer thickneses and doping used in the IMPATT diode (2) is selected to generate a desired level of tunnel current at the peak reverse bias voltage applied to the diode (2).

The narrow bangap region (4) makes it easier for electrons to tunnel from the valence band (V) to the conduction band (C) and is effective to inject electrons into the conduction band of the wide bandgap region (10) in a predictable manner. This is shown by the arrow in Figure 2. The electrons injected into the wider bandgap region (10) then undergo avalanche multiplication in the avalanche region (10).

An n-type doping spike (18) separates the low doped region (10) and the low doped region (12) and so forms the boundary between the avalanche region (10) and the drift region (12) of the device (2).

The avalanche region is the region where the impact ionisation is significant and will extend into region (8) although it is unlikely to include all of region (8). As can be seen from Figure 2 the narrow bandgap region (4) is located within the conventional avalanche region and can be considered as part of the avalanche region.

The p^{++} and n^{++} contact regions should have sufficiently high doping levels to form good Ohmic contacts with the metalisation layer of the diode, as is well known in the art. Alternative contact technologies could be used, e.g. the p^{++} region could be replaced by an n^{+} region to form a Shottky barrier with the metalisation layer.

Figure 2 shows the variation in conduction band (C) and valence band (V) edge energies along the IMPATT diode of Figure 1. This is similar to that of a conventional lo-hi-lo diode except for the narrow bandgap region (4) which makes it easier for an electron to tunnel from the valence band to the conduction band at applied reverse bias voltages above the breakdown voltage in order to inject electrons into the region (10). This tunnelling is indicated by the arrow in Figure 2. The gradual reduction in energy of the valence and conduction bands, from left to right in Figure 2, across the intrinsic region (10) means that electrons injected into the intrinsic region (10) undergo avalanche multiplication. It can be seen that the n-type doping spike (18) terminates the avalanche region of the device (2).

The length of the drift region (12) L_D and the length of the avalanche region (L_A) are chosen such that in the fundamental mode of rf oscillation across the electrodes (22) and (24), the period of oscillation (P) of the fundamental mode is between 4 and 12 times, and preferably close to 8 times the avalanche region transit time (T_A), ie. the time it takes for an electron to transit the avalanche region (10). It has been found that this substantially reduces the noise generated by an IMPATT diode. This applies to conventional IMPATT diodes as well as to IMPATT diodes having a narrow bandgap region.

If the fundamental mode of rf voltage oscillation (having a period of oscillation P) begins at t=0, as shown in Figure 6, then an IMPATT diode is generally designed so that the current from the avalanche region

enters the drift region (12) after a time t=P/2 (t=4T in Figure 6), ie. when the fundamental mode of voltage oscillation (V) ends its positive voltage half cycle. In order to achieve maximum negative resistance IMPATT diodes are generally designed so that the transit time through the drift region is close to P/2. Accordingly, the length of the drift region is generally chosen to be $L_D=V_SP/2$, where V_S is the saturated electron drift velocity. The length of the avalanche region will be $L_A=T_A/V_S$,, where T_A is the time it takes for an electron to transit the avalanche region, ie. the avalanche region transit time.

Thus when $P=8T_A$, then because $L_D=V_SP/2$ and $T_A=L_A/V_S$ as discussed above, this leads to the relationship;

$$L_D=4T_AV_S=4L_A,$$

that is, the drift region length L_D is 4 times the avalanche region length L_A. It has been found that this substantially reduces the noise generated by an IMPATT diode according to the present invention.

To demonstrate the principle of the present invention a Silicon Germanium/Silicon based structure according to Figure 1 has been simulated. Where the fraction of Germanium in the Silicon Germanium alloy is denoted by x, the narrow bandgap region (4) was made of a 200A (Angstrom) thick layer of Silicon Germanium with x=0.33. The low doped region (8,10) was made of a 2000A thick layer of intrinsic Silicon. To reduce the strain in the Silicon Germanium layer (4) for stable operation at high power it may be necessary to add Carbon to the Silicon Germanium alloy. For this particular alloy layer thickness and composition it was found that including the Silicon Germanium layer (4) as the first part of an intrinsic avalanche layer (8,10) as indicated in Figure 1 gave a satisfactorily high tunnel current. The magnitude and thickness of the doping spike (18) was chosen to give an average

electric field in the avalanche region (10) of $5x10^5$V/cm. The amplitude of the time variation of the field was taken as 50% of the average field (ie. A=0.5 see below) which gave a peak tunnel current of approximately 1.5amps/cm^2.

Where the narrow band gap region (4) is SiliconGermanium (SiGe) the injection of tunnel current will use the indirect SiGe bandgap. Semiconductor materials, such as, GaAs/AlGaAs or InGaAs/InP or other hetero systems could be used to implement the device (2) shown in Figure 1 such that a tunnel current is injected into the avalanche region at peak reverse bias. Si has the advantage of high thermal conductivity and demonstrated performance at high frequencies up to 300GHz.

The device (2) is reverse biased by applying a constant reverse bias voltage across electrodes (22) and (24) which voltage is close to the reverse bias breakdown voltage of the device. In addition an oscillating voltage variation is generated across the electrodes (22) and (24) by locating the diode (2) in a microwave cavity and appropriately tuning the cavity. As is well known in the art alternative resonant circuits may be used. The inclusion of the narrow band gap region (4) ensures that a relatively high tunnel current is injected into the avalanche region (16) at the peak reverse bias voltage.

Without the narrow bandgap region this injection arises from the reverse saturation current which normally has very low values such that the number of particles available to initiate an avalanche is low, often less than 1, with consequent high statistical fluctuation. The tunnel current is designed to be much higher, yielding much lower noise prior to avalanche.

The tunnel current consists of electrons and holes, and referring to Figure 1, the electrons flow into the avalanche region (10) and the holes

flow into the p^{++} region (8). The electrons flowing into the avalanche region (10) then generate electrons and holes in the Si avalanche region (10) by impact ionisation.

The injected tunnel current is generated entirely in the SiGe narrow bandgap region (4) and comprises a narrow pulse of charge carriers close to the peak reverse bias voltage which pulse of charge carriers is then injected into the Si avalanche region (10). The relatively narrow pulse of injected tunnel current has low statistical fluctuation and will initiate a very low noise avalanche multiplication in the avalanche region (10). The structure of the diode (2) enables a relatively high tunnel current to be injected into the avalanche region (10). Also, because the inclusion of the narrow bandgap region (4) makes it easier for electrons to move from the valence band (V) into the conduction band (C) the diode (2) can be operated at lower electric fields and multiplication values than for a conventional lo-hi-lo type IMPATT diode with similar power outputs. This will yield an improvement in reliability and efficiency.

As indicated above in a preferred embodiment, the narrow bandgap layer (4) is made of a 200A thick layer of 33% Silicon Germanium and the avalanche region (8,10) is made of a 2000A thick layer of Silicon. The fundamental oscillation of the voltage (V) generated across the device (2) will take the form;

$$V = V_0[1+A\cos(\omega t)]$$

with A = a constant multiplier which is less than 1,

V_0 = a reverse bias voltage close to the breakdown voltage, and

$V_0 A \cos(\omega t)$ = a sinusoidal voltage,

as is described above. In this case the tunnel current shown in Figure 5 is obtained. In Figure 5 the phase origin of the horizontal axis (ie. phase = 0) is chosen to correspond to the peak reverse bias voltage applied across the electrodes (22) and (24). This peak reverse bias occurs at t=2T on Figure 6, at a 90° phase lag relative to the origin of the rf voltage oscillation at t=0 on Figure 6. The tunnel current is generated entirely in the narrow bandgap region (4) and forms a pulse close to the peak reverse bias voltage which is then injected into the Si avalanche region (10). From Figure 5, it is expected that the tunnel current will approach 1.6 amp/cm^2 in the structure of Figure 2 and should give very low noise avalanche multiplication.

It will be understood by the person skilled in the art that the magnitude of the tunnel current shown in Figure 5 can be varied by changing the thickness or alloy composition of the narrow bandgap layer (4), possibly using multi-quantum wells to alleviate strain. It is also possible to design the doping profile or to use doping spikes to change the electric field across the narrow bandgap region (4) relative to the field across the avalanche region (10).

The origin of phase is defined as the point at which the rf voltage is zero and about to rise (ie. t=0 in Figure 6). The peak tunnel current coincides with the peak electric field which occurs at a phase of 90° (ie. t=2T in Figure 6). The avalanche multiplication is arranged so the total current (ie. tunnel plus avalanche current - I in Figure 6) normally peaks close to a phase of 180° (ie. t=4T in Figure 6) at which the oscillating rf voltage passes through zero to become negative.

As indicated above, the device (2) is reverse biased to just below the breakdown voltage and a periodic voltage is generated across the electrodes (22) and (24). Thus, towards the peak of the positive half cycle of the sinusoidal voltage, the voltage generated across the

electrodes (22) and (24) is greater than the breakdown voltage. The avalanche noise is suppressed most effectively when the period of oscillation of the fundamental mode of voltage oscillation is approximately eight times the avalanche zone transit time, ie. eight times the time it takes a charge carrier to pass through the avalanche zone (10).

In Figure 4 is shown a graph of the computed noise of a device (2) as a function of the multiplication factor of the avalanche region (10) for various periods of oscillation of the sinusoidal voltage applied across the electrodes (22) and (24). The device simulated was a Silicon lo-hi-lo diode having the structure shown in Figure 1 and having a 0.3 micron thick avalanche region (10) with a Silicon Germanium narrow bandgap layer. It can be seen from the Figure 4 graph that the noise at high multiplication levels is reduced when the period of oscillation approaches eight times the avalanche zone transit time, ie. $P=8T_A$ (indicated as P=8 in Figure 4). The excess noise factor at $P=8T_A$ decreases as the multiplication factor increases and can achieve almost noise free multiplication.

In Figure 6 is plotted the total current waveform (I) consisting of tunnel current and avalanche current for the device of Figure 2 when the sinusoidal voltage (V), also shown in Figure 6, has a period of P=8T. The current (I) starts to rise at time t=2T which corresponds to the peak reverse bias voltage (V) of the applied sinusoidal voltage applied across the electrodes (22) and (24) of the device (2). The total current (I) goes through a maximum close to t=4T which corresponds to the time at which the sinusoidal voltage (V) becomes negative.

By using relatively high tunnel currents, efficient power generation should be possible with relatively low multiplication factors, so that the

device (2) can be operated with a lower voltage drop across the avalanche zone. This should improve both efficiency and reliability.

Figure 3 shows the variation in conduction band (C) and valence band (V) edge energies for the device of Figure 1 (assuming Silicon Germanium as the narrow bangap region), except that in this case injection of electrons from the valence band and into the conduction band occurs by optical excitation (represented by arrow α of Figure 3) of the electrons in the narrow bandgap layer as well as by electron tunnelling (represented by arrow β of Figure 3). If electromagnetic radiation with an energy greater than the bandgap of the narrow bandgap material (4) is incident on the narrow bandgap region (4), electrons in the valence band (V) of the narrow bandgap region can absorb a photon (26) of the electromagnetic radiation and jump into the conduction band (C). Excitation in the narrow bandgap region could be done by horizontal access (wave guide) geometries to enhance optical absorption. The narrow bandgap region (4) makes it easier for an electron to jump from the valence band to the conduction band in order to inject electrons into the avalanche region (10). This optical excitation is indicated by the arrow α in Figure 3.

Doping spikes can be used to adjust the electric field across the narrow bandgap layer to achieve the desired ratio of the injection current generated by optical excitation to the injection current generated by tunnelling. There is then a potential for optical injection locking of isolated diodes or arrays of diodes of the type shown in Figure 1 and optical control of the phase and amplitude of the signal output from the diode (2).

Alternatively, as is shown in Figure 9, the narrow bandgap region (4') can be adjacent to but outside of the avalanche region (10'). In this

case a doped region (8') will be required between the narrow bandgap region (4') and the avalanche region (10') in order to change the relative electric fields.

The above description has related to single drift diodes as shown in Figure 1, but the present invention can also be applied to double drift diodes, such as that shown in Figures 7a and 8a. The diodes shown in Figure 7a and 8a are fabricated from a Gallium Arsenide/Aluminium Gallium Arsenide structure

The double drift IMPATT diodes shown in Figures 7a and 8a have heavily doped p^{++} region (42), low doped semiconductor regions (44), (46) and (48) and a heavily doped n^{++} region (50). Region (46) comprises the avalanche region and regions (44) and (48) comprise the two drift regions. A p-type doping spike (54) and an n-type doping spike (56) separate the avalanche region (46) from the drift regions (44) and (48). In the diode shown in Figure 7a a Gallium Arsenide narrow bandgap region (40) is located in the centre of the avalanche region (46). In the diode shown in Figure 8a a Gallium Arsenide narrow bandgap region (52) is located to the left hand side of the avalanche region (46). As described above in relation to the single drift diode of Figure 1, the narrow bandgap regions (40) and (52) make it easier for electrons to tunnel from the valence band (V) to the conduction band (C) in order to reliably inject a tunnel current into the avalanche region.

The material compositions, layer thickness and doping used in the structures of Figure 7a and 8a are selected to generate a desired level of tunnel current at peak reverse bias voltage and appropriate electric field levels in the avalanche region to ensure a desired avalanche multiplication by impact ionisation and in the drift regions to ensure that carriers achieve saturation velocity. As indicated above it is preferred that each drift region (44) and (48) has a length approximately four

times the length of the avalanche region (46). Thus, in the fundamental mode of oscillation the period of the fundamental oscillation will be approximately eight times the transit time of the avalanche region, as discussed above in relation to the diode of Figure 1.

Figures 7b and 8b show the variation in conduction band (C) and valence band (V) edge energies along the IMPATT diodes of Figures 7a and 8a respectively. These are similar to the conduction and valence band edge energies of a conventional double drift diode except for the edge energies at the respective narrow bandgap regions (40) and (52).

CLAIMS

1. An impact ionisation avalanche transit time (IMPATT) diode device (2) comprising a main avalanche region (10, 46) and a drift region (12, 44, 48), characterised in that the device additionally comprises a narrow bandgap region (4, 40) with a bandgap narrower than the bandgap in the main avalanche region (10, 46) which narrow bandgap region (4, 40) is located adjacent to the main avalanche region (10,46) in order to generate within the narrow bandgap region (4, 40) a tunnel current which is injected into the main avalanche region (10,46).

2. An IMPATT diode according to claim 1 wherein the narrow bandgap region (4, 40) is arranged to generate a tunnel current for injection into the main avalanche region (10, 46) at the peak reverse bias voltage applied to the diode.

3. An IMPATT diode according to claim 1 or claim 2 wherein the narrow bandgap region (4, 40) is located at the edge of the main avalanche region (10, 46).

4. An IMPATT diode according to any one of the preceding claims wherein the narrow bandgap region (4) is located between a heavily doped contact region (8) and the main avalanche region (10).

5. An IMPATT diode according to any one of the preceding claims wherein the narrow bandgap region (4, 40) comprises one layer of narrow bandgap material.

6. An IMPATT diode according to any one of claims 1 to 4 wherein the narrow bandgap region (4, 40) comprises a plurality of layers of narrow bandgap material.

7. An IMPATT diode according to any one of the preceding claims wherein the diode has a lo-hi-lo doping profile.

8. An IMPATT diode according to claim 7 wherein the diode is a Misawa p-i-n diode.

9. An IMPATT diode according to any one of claims 1 to 6 wherein the diode is a double drift diode.

10. An IMPATT diode according to any one of the preceding claims wherein the diode is made of III-V semiconductor materials.

11. An IMPATT diode according to any one of claims 1 to 7 wherein the diode is made of group IV semiconductor materials.

12. An IMPATT diode according to claim 11 wherein the narrow bandgap region (4, 40) is made of at least one layer of Silicon Germanium and the main avalanche region (10, 46) is made of Silicon.

13. An IMPATT diode according to claim 10 wherein the narrow bandgap region (4, 40) is made of at least one layer of Gallium Arsenide and the main avalanche region (10, 46) is made of Aluminium Gallium Arsenide.

14. An IMPATT diode according to any one of the preceding claims wherein the length of the drift region or regions (12, 44, 48) is between 2 and 6 times the length of the avalanche region (10, 46).

15. An IMPATT diode according to claim 14 wherein the length of the drift region or regions (12, 44, 48) is between 3.5 and 4.5 times the length of the avalanche region (10, 46).

16. An IMPATT diode according to any one of the preceding claimed arranged such that at least part of the tunnel current can be generated by optical excitation.

17. A method of operating an IMPATT diode according to any one of the preceding claims such that an oscillating voltage across the diode has a period of between 4 and 12 times the transit time of the avalanche region (10, 46).

18. A method according to claim 17 wherein the oscillating voltage has a period of between 7.5 and 8.5 times the transit time of the avalanche region (10, 46).

19. A method of operating an IMPATT diode according to any one of claims 1 to 17 including the step of optically exiting at least part of the tunnel current.

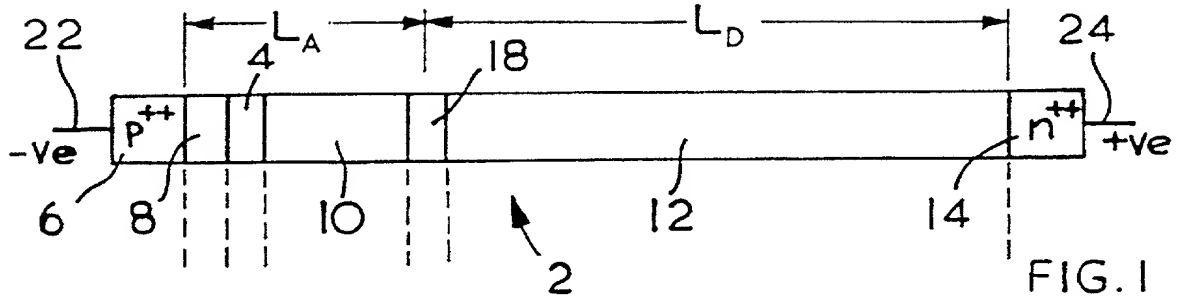


FIG.1

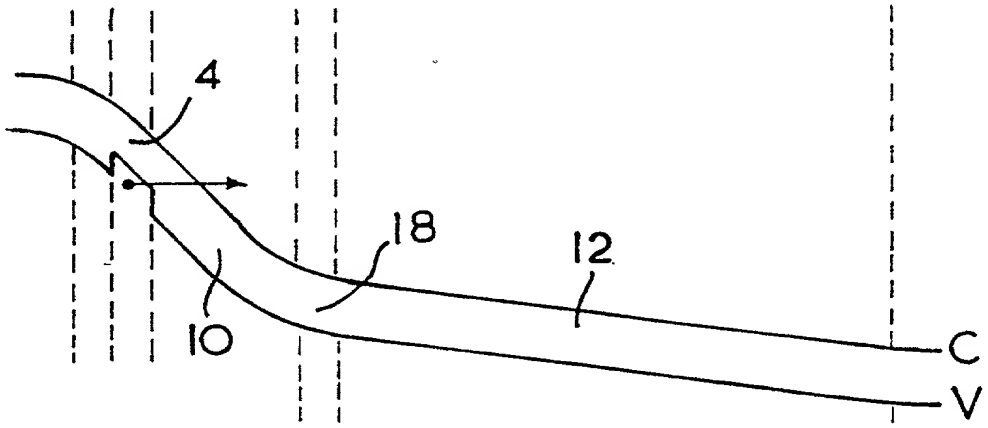


FIG.2

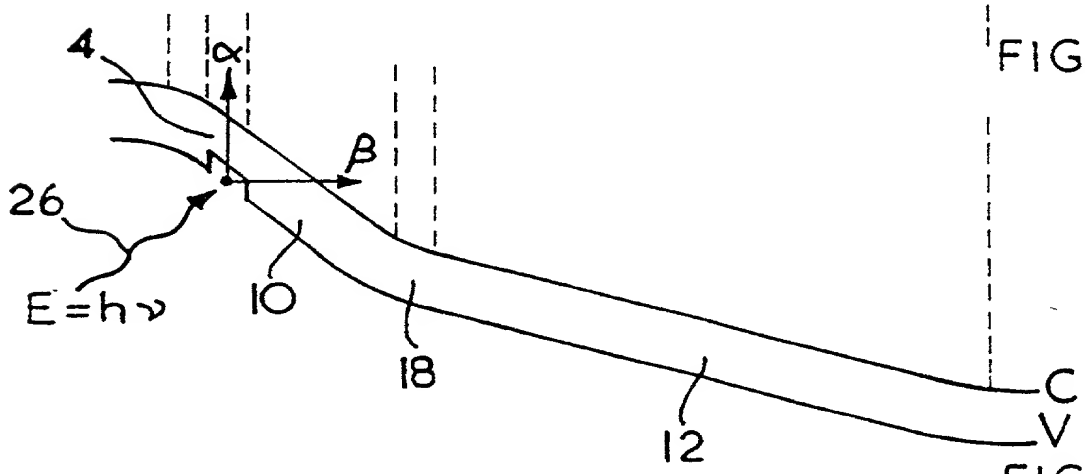


FIG.3

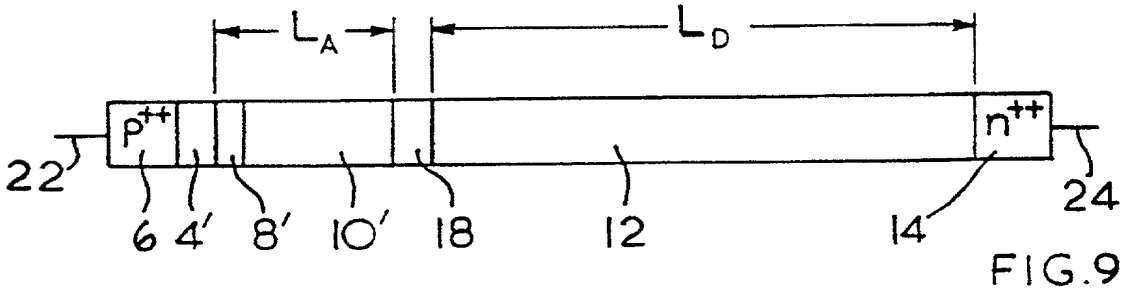


FIG.9

FIG. 4

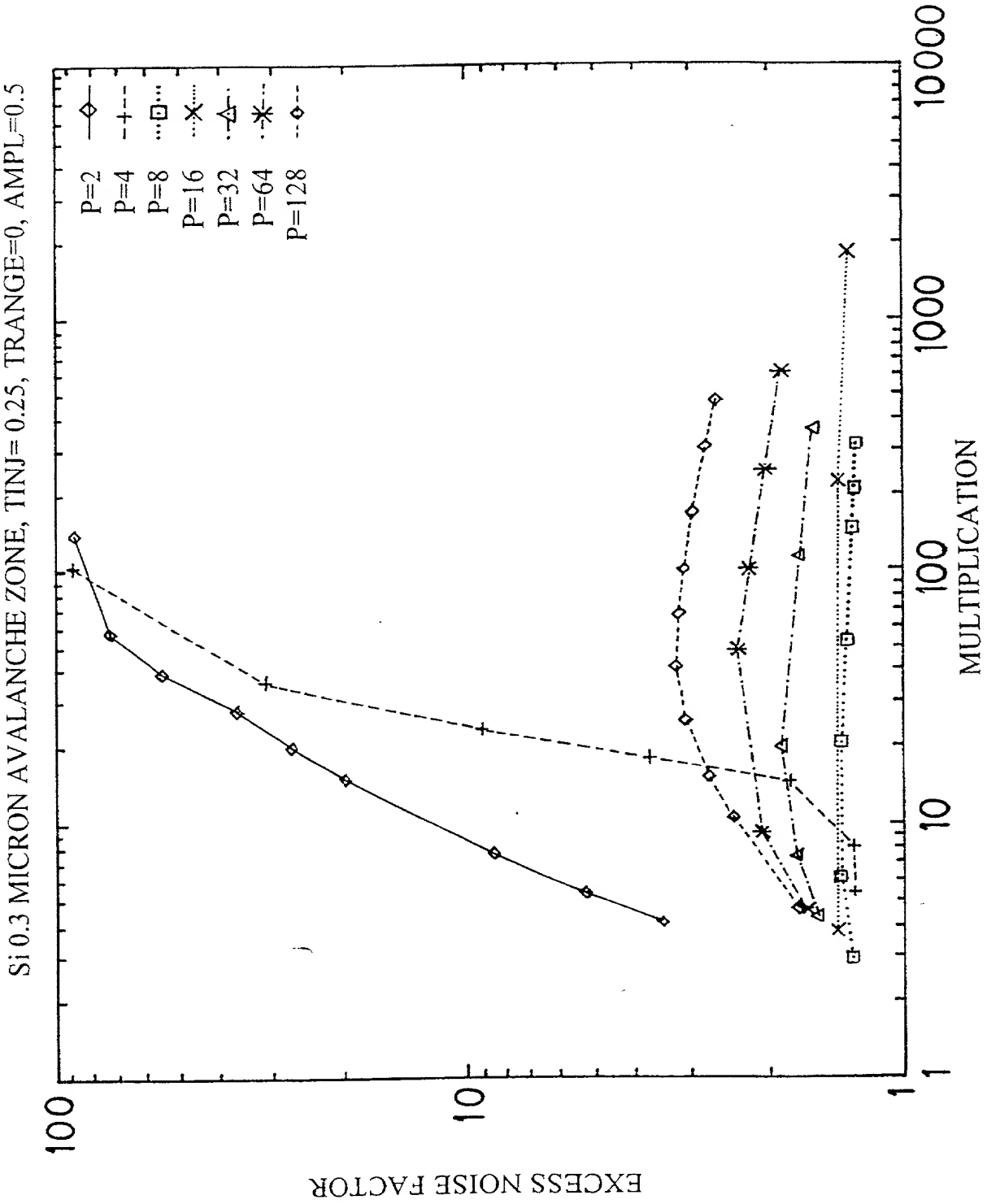
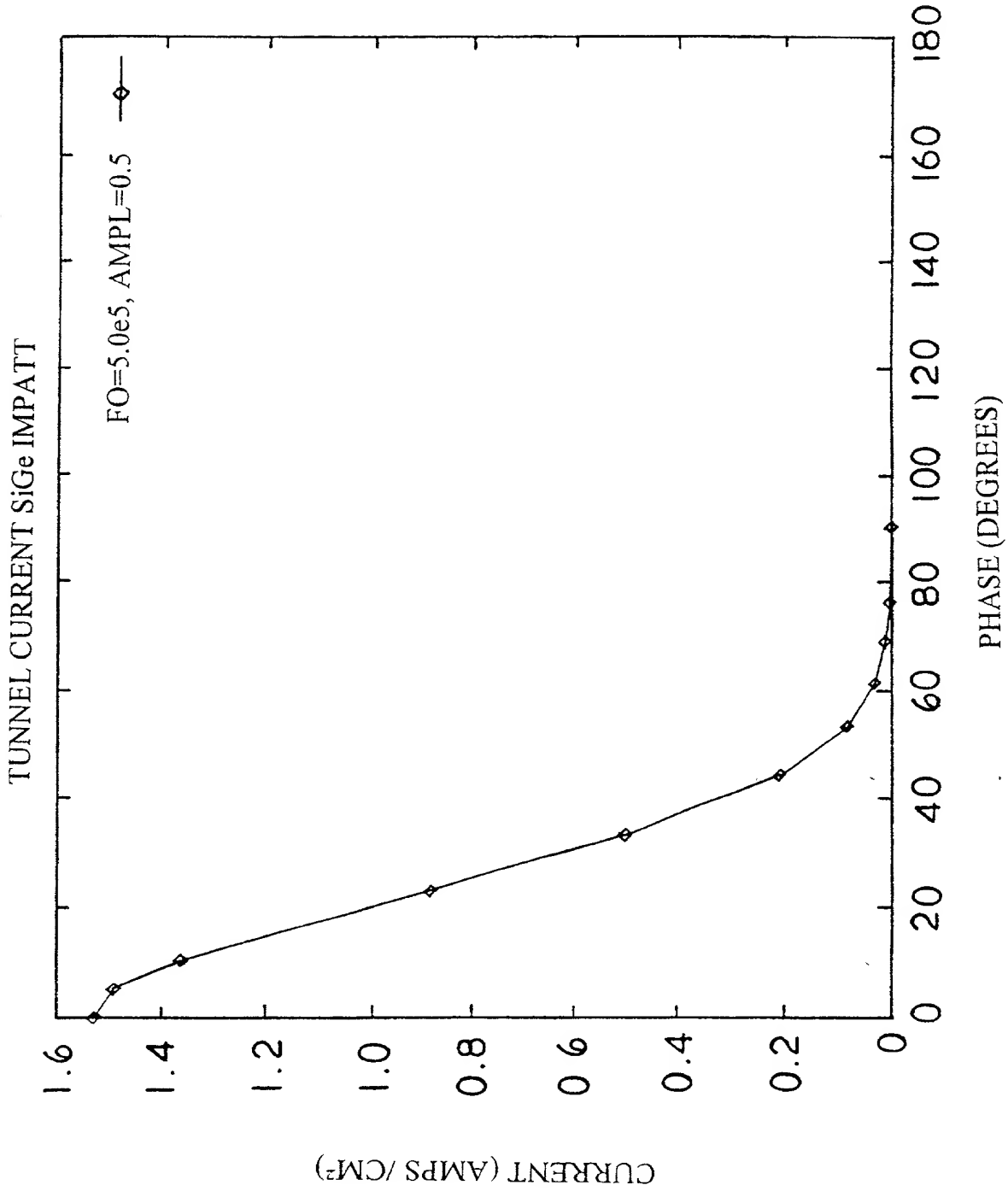

Si 0.3 MICRON AVALANCHE ZONE, TINJ= 0.25, TRANGE=0, AMPL=0.5
P=2
P=4
P=8
P=16
P=32
P=64
P=128
EXCESS NOISE FACTOR
100
10
1
MULTIPLICATION
1
10
100
1000
10000

FIG.5


TUNNEL CURRENT SiGe IMPATT
FO=5.0e5, AMPL=0.5
CURRENT (AMPS /CM²)
PHASE (DEGREES)
0
0.2
0.4
0.6
0.8
1.0
1.2
1.4
1.6
0
20
40
60
80
100
120
140
160
180

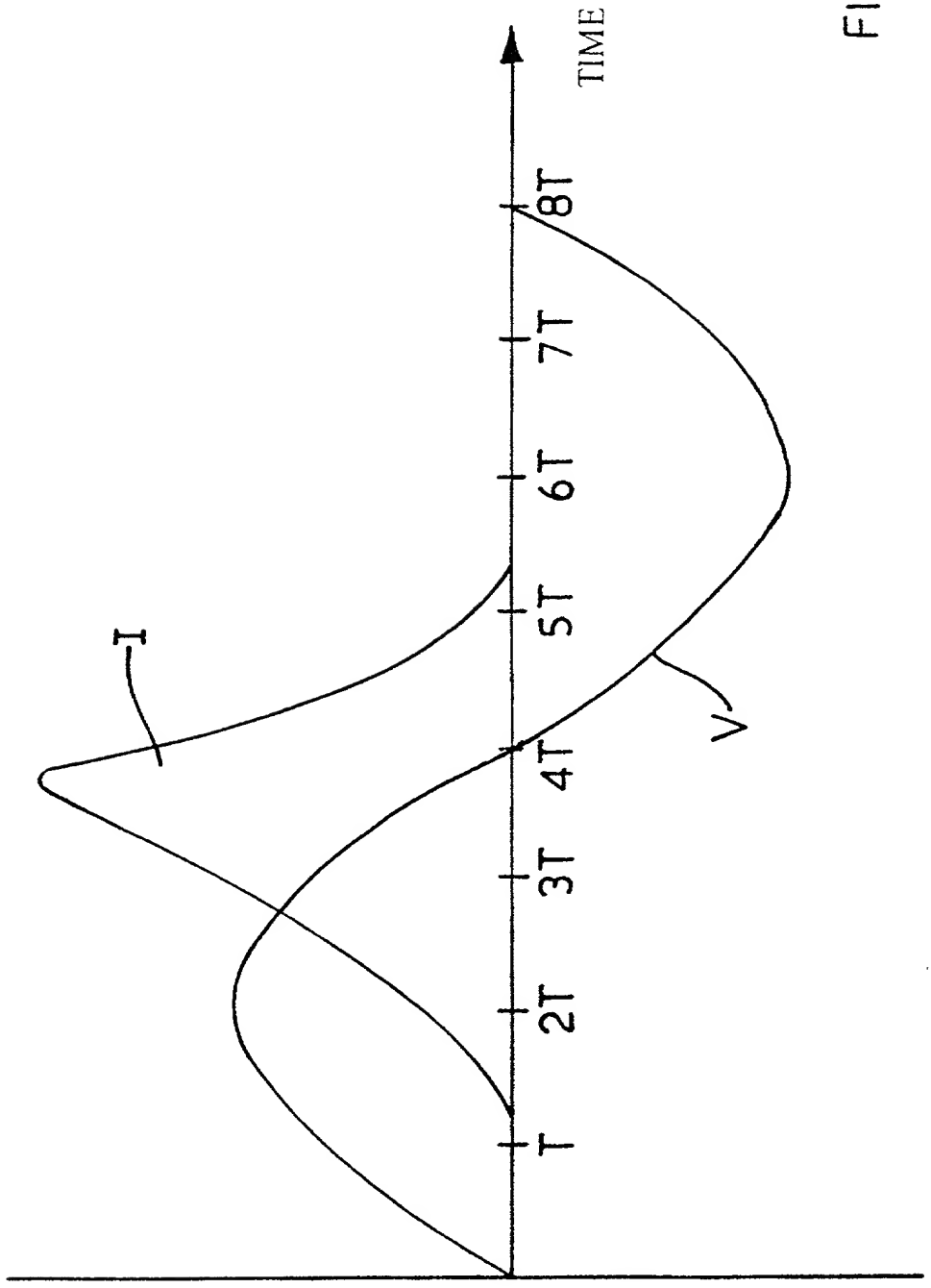


FIG. 6

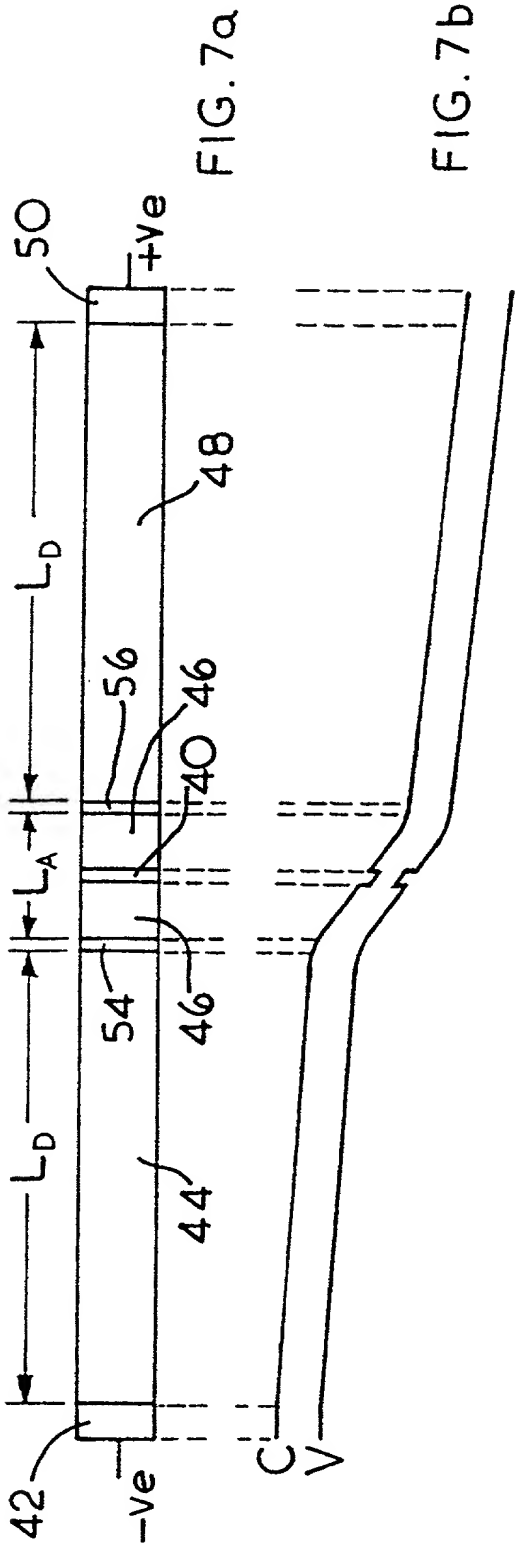


FIG. 7a

FIG. 7b

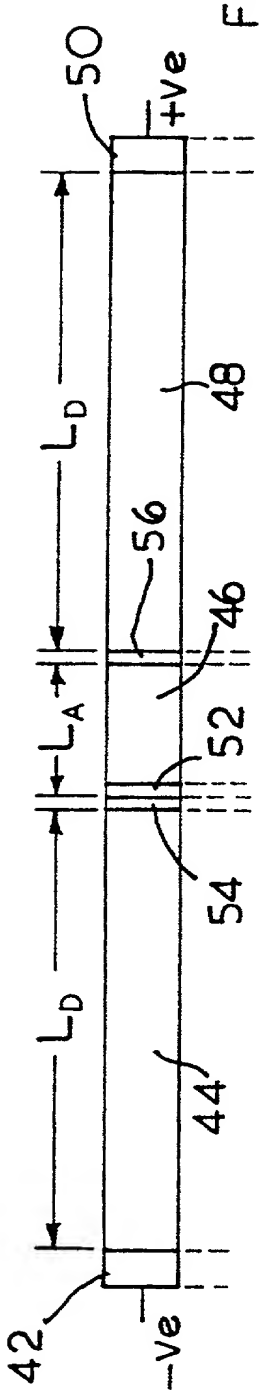


FIG. 8a

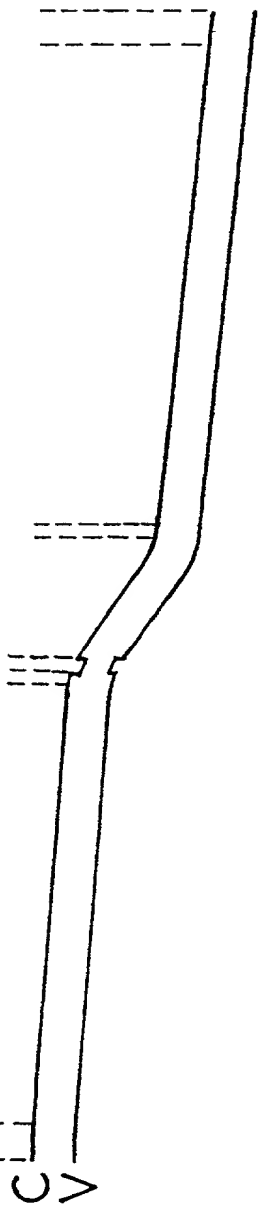


FIG. 8b

RULE 63 (37 C.F.R. 1.63)
DECLARATION AND POWER OF ATTORNEY
FOR PATENT APPLICATION
IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

As a below named inventor, I hereby declare that my residence, post office address and citizenship are as stated below next to my name, and I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

Improvements in IMPATT Diodes

the specification of which (**check** applicable **box(s)**):

☐ is attached hereto

☐ was filed on _____ as U.S. Application Serial No. _____

☒ was filed as PCT international application No. PCT/GB99/03428 on 22/10/1999

and (if applicable to U.S. or PCT application) was amended on 05/10/2000

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above. I acknowledge the duty to disclose information which is material to the patentability of this application in accordance with 37 C.F.R. 1.56. I hereby claim foreign priority benefits under 35 U.S.C. 119/365 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed or, if no priority is claimed, before the filing date of this application:

Priority Foreign Application(s):

Application Number	**Country**	**Day/Month/Year Filed**
9823115.2	GB	23/10/1998

I hereby claim the benefit under 35 U.S.C. §119(e) of any United States provisional application(s) listed below.

Application Number	**Date/Month/Year Filed**

I hereby claim the benefit under 35 U.S.C. 120/365 of all prior United States and PCT international applications listed above or below and, insofar as the subject matter of each of the claims of this application is not disclosed in such prior applications in the manner provided by the first paragraph of 35 U.S.C. 112, I acknowledge the duty to disclose material information as defined in 37 C.F.R. 1.56 which occurred between the filing date of the prior applications and the national or PCT international filing date of this application:

Prior U.S./PCT Application(s): Application Serial No.	**Day/Month/Year Filed**	**Status: patented pending, abandoned**
PCT/GB99/03428	22/10/1999	PENDING

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon. And I hereby appoint **NIXON & VANDERHYE P.C., 1100 North Glebe Rd., 8th Floor, Arlington, VA 22201-4714, telephone number (703) 816-4000 (to whom all communications are to be directed)**, and the following attorneys thereof (of the same address) individually and collectively my attorneys to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith and with the resulting patent: Arthur R. Crawford, 25327; Larry S. Nixon, 25640; Robert A. Vanderhye, 27076; James T. Hosmer, 30184; Robert W. Faris, 31352; Richard G. Besha, 22770; Mark E Nusbaum, 32348; Michael J. Keenan, 32106; Bryan H. Davidson, 30251; Stanley C. Spooner, 27393; Leonard C. Mitchard, 29009; Duane M. Byers, 33363; Jeffry H. Nelson, 30481; John R. Lastova, 33149; H. Warren Burnam, Jr. 29366; Thomas E. Byrne, 32205; Mary J. Wilson, 32955; J. Scott Davidson, 33489; Alan M. Kagen, 36178; William J. Griffin, 31260; Robert A Molan, 29834; B. J. Sadoff, 36663; James D. Berquist, 34776; Updeep S. Gill, 37334; Michael J. Shea, 34725; Donald L. Jackson, 41090; Michelle N. Lester, 32331.*

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1-00

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2. Inventor's Signature: _____ Date: _____

Inventor: Robert (first) G MI DAVIS (last) GB (citizenship)

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FOR ADDITIONAL INVENTORS, check box ☐ and attach sheet with same information and signature and date for each.

RULE 63 (37 C.F.R. 1.63)
DECLARATION AND POWER OF ATTORNEY
FOR PATENT APPLICATION
IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

As a below named inventor, I hereby declare that my residence, post office address and citizenship are as stated below next to my name, and I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

Improvements in IMPATT Diodes

the specification of which **(check** applicable **box(s))**:

☐ is attached hereto

☐ was filed on _____ as U.S. Application Serial No. _____

☒ was filed as PCT International application No PCT/GB99/03428 on 22/10/1999

and (if applicable to U.S. or PCT application) was amended on 05/10/2000

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above. I acknowledge the duty to disclose information which is material to the patentability of this application in accordance with 37 C.F.R. 1.56. I hereby claim foreign priority benefits under 35 U.S.C. 119/365 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed or, if no priority is claimed, before the filing date of this application:

Priority Foreign Application(s):

Application Number	Country	Day/Month/Year Filed
9823115.2	GB	23/10/1998

I hereby claim the benefit under 35 U.S.C. §119(e) of any United States provisional application(s) listed below.

Application Number	Date/Month/Year Filed

I hereby claim the benefit under 35 U.S.C. 120/365 of all prior United States and PCT international applications listed above or below and, insofar as the subject matter of each of the claims of this application is not disclosed in such prior applications in the manner provided by the first paragraph of 35 U.S.C. 112, I acknowledge the duty to disclose material information as defined in 37 C.F.R. 1.56 which occurred between the filing date of the prior applications and the national or PCT international filing date of this application:

Prior U.S./PCT Application(s): Application Serial No.	Day/Month/Year Filed	Status: patented pending, abandoned
PCT/GB99/03428	22/10/1999	PENDING

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon. And I hereby appoint **NIXON & VANDERHYE P.C., 1100 North Glebe Rd., 8th Floor, Arlington, VA 22201-4714, telephone number (703) 816-4000 (to whom all communications are to be directed)**, and the following attorneys thereof (of the same address) individually and collectively my attorneys to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith and with the resulting patent: Arthur R. Crawford, 25327; Larry S. Nixon, 25640; Robert A. Vanderhye, 27076; James T. Hosmer, 30184; Robert W. Faris, 31352; Richard G. Besha, 22770; Mark E. Nusbaum, 32348; Michael J. Keenan, 32106; Bryan H. Davidson, 30251; Stanley C. Spooner, 27393; Leonard C. Mitchard, 29009; Duane M. Byers, 33363; Jeffry H. Nelson, 30481; John R. Lastova, 33149; H. Warren Burnam, Jr. 29366, Thomas E. Byrne, 32205; Mary J. Wilson, 32955; J. Scott Davidson, 33489; Alan M. Kagen, 36178; William J. Griffin, 31260; Robert A. Molan, 29834; B. J. Sadoff, 36663; James D. Berquist, 34776; Updeep S. Gill, 37334; Michael J. Shea, 34725; Donald L. Jackson, 41090; Michelle N. Lester, 32331.*

27

1. Inventor's Signature: _____ Date: _____

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FOR ADDITIONAL INVENTORS, check box ☐ and attach sheet with same information and signature and date for each.